CLAIMS

What is claimed is:

1. A printed circuit board (PCB) comprising:

a first multilayered portion including at least one dielectric layer and at least one conductive plane wherein said conductive plane includes signal lines capable of having signals pass therealong at a first frequency; and

a second multilayered portion bonded to said first multilayered portion and adapted for having a plurality of electronic components electrically coupled thereto, said second multilayered portion including at least one dielectric layer and at least one conductive signal plane wherein said conductive signal plane of said second multilayered portion includes signal lines capable of having signals pass therealong at a higher frequency than said first frequency to thereby provide a high speed connection between at least two of said electrical components.

2. The PCB of claim 1 wherein said second multilayered portion includes a conducting plane, first and second dielectric layers on opposite sides of said conducting plane, and the number of conductive signal plans is two, each conductive signal plane including said signal lines capable of having signals pass therealong and being positioned on a respective one of said first and second dielectric layers opposite said conducting plane.

3. The PCB of claim 2 wherein said second multilayered portion further includes a conductive through hole interconnecting at least one of said signal lines of said conductive signal plane on said first dielectric layer with at least one of said signal lines of said conductive signal plane on said second dielectric layer.

4. The PCB of claim 2 further including a third dielectric layer positioned on said second dielectric layer and said conductive signal plane positioned thereon having said signal lines capable of having signal pass therealong, said third dielectric layer including at least one opening therein exposing at least one of said signal lines such that at least one of said electrical components can be electrically coupled thereto.

5. The PCB of claim 4 wherein said at least one opening includes a layer of conductive material.

6. The PCB of claim 4 wherein said second multilayered portion includes a conductive through hole interconnecting at least one of said signal lines of said conductive signal plane on said first dielectric layer with at least one of said signal lines of said conductive signal plane on said second dielectric layer, said at least one signal line of said conductive signal plane on said first dielectric layer being said at least one signal line exposed by said opening in said third dielectric layer.

7. The PCB of claim 4 further including a conductive plane located on said third dielectric layer.

8. The PCB of claim 7 further including a fourth dielectric layer positioned on said third dielectric layer and on said conductive plane located on said third dielectric layer, said fourth dielectric layer including at least one opening therein exposing said at least one opening in said third dielectric layer.

9. The PCB of claim 8 wherein said both of said at least one openings in said third and fourth dielectric layers includes a layer of conductive material thereon, said layers of conductive material being electrically coupled together, said at least one of said electrical components adapted for being electrically coupled to said layer of conductive material in said at least one opening in said fourth dielectric material.

10. The PCB of claim 1 wherein said at least one dielectric layer in said second multilayered portion has a lower dielectric constant than said at least one dielectric layer in said first multilayered portion.

11. The PCB of claim 1 wherein said at least one dielectric layer in said second multilayered portion has a lower loss factor than said at least one dielectric layer in said first multilayered portion.

12. The PCB of claim 1 wherein the signal rate of said high speed connection in said second multilayered portion is from about three to about ten gigabits per second.

13. A method of making a PCB, said method comprising:

providing a first multilayered portion including at least one dielectric layer and at least one conductive plane wherein said conductive plane includes signal lines capable of having signals pass therealong at a first frequency;

providing a second multilayered portion adapted for having a plurality of electronic components electrically coupled thereto, said second multilayered portion including at least one dielectric layer and at least one conductive signal plane wherein said conductive signal plane of said second multilayered portion includes signal lines capable of having signals pass therealong at a higher frequency than said first frequency to thereby provide a high speed connection between at least two of said electrical components; and

bonding said first and second multilayered portions to form said PCB.

14. The method of claim 13 further including providing a conductive through hole within said second multilayered portion prior to said bonding of said first and second multilayered portions.

15. The method of claim 13 wherein said bonding is accomplished by lamination.

16. An information handling system comprising a PCB including a first multilayered portion including at least one dielectric layer and at least one conductive plane wherein said conductive plane includes signal lines capable of having signals pass therealong at a first frequency, and a second multilayered portion bonded to said first multilayered portion and adapted for having a plurality of electronic components electrically coupled thereto, said second multilayered portion including at least one dielectric layer and at least one conductive signal plane wherein said conductive signal plane of said second multilayered portion includes signal lines capable of having signals pass therealong at a higher frequency than said first frequency to thereby provide a high speed connection between at least two of said electrical components.